1. A method for packaging a MEMS device comprising:

providing a first substrate having a functional element and metal leads thereon and a second SOI substrate having at least one recessed cavity in a first silicon portion thereof with metal connectors therein;

bonding a surface of the first substrate to a non-recessed surface of the first silicon portion of the second SOI substrate and bonding the metal leads of the first substrate to respective metal connectors of the second SOI substrate to enclose and seal the functional element of the first substrate within the recessed cavity of the second SOI substrate; and

forming metal pads on each of the metal connectors of the second SOI substrate through the second SOI substrate for feeding electrical signals to and from the functional element of the first substrate sealed in the cavity of the second SOI substrate through the metal leads, the connectors and the pads.

2. The method of claim 1 wherein the recessed cavity is provided with a depth greater than the thickness of the functional element and less than the combined thickness of the metal leads and the respective metal connectors prior to bonding.

3. The method of claim 1 wherein the second SOI substrate comprises the first silicon portion, a second silicon portion, and an intermediate oxide layer buried between the first silicon portion and second silicon portion, and the method further comprises, after bonding, removing the second silicon portion leaving the oxide layer exposed.

4. The method of claim 3 further comprising, after forming, depositing a passivation layer on the exposed oxide layer and metal pads.

5. The method of claim 4 wherein depositing the passivation layer includes plasma enhanced chemical vapor deposition with a nitrogen-containing reactant to deposit a nitride passivation layer.

6. The method of claim 1 wherein bonding comprises room temperature fusion bonding.

7. The method of claim 6 wherein the fusion bonding includes applying a pressure in the range of about 800-1400 pounds.

8. The method of claim 6 wherein the first substrate is a silicon base wafer.

9. The method of claim 1 wherein bonding comprises anodic bonding.

10. The method of claim 9 wherein the anodic bonding comprises applying an electrical bias in the range of about 100-1000 V and a temperature in the range of about 300-500°C.

11. The method of claim 9 wherein the first substrate is a Pyrex glass base wafer.

12. The method of claim 1 wherein the metal leads and the metal connectors each comprise a metal selected from the group consisting of: aluminum, gold, aluminum alloys and gold alloys.

13. The method of claim 12 wherein the metal leads and connectors comprise the same metal.

14. The method of claim 1 wherein the forming metal pads comprises depositing aluminum on a titanium/titanium nitride liner.

15. The method of claim 1 wherein the forming metal pads comprises depositing gold on a chromium liner.

16. The method of claim 1 wherein the second SOI substrate comprises a plurality of recessed cavities each having at least one metal connector therein, the functional element being enclosed and sealed within one of the plurality of cavities, and the metal pads on each of the metal connectors connecting over the second SOI substrate.

17. The method of claim 16 further comprising forming a plurality of functional elements, each enclosed and sealed within one of the plurality of cavities.

18. The method of claim 1 further comprising, before bonding, growing an oxide on the non-recessed surface and in the recessed cavity of the first silicon portion, and thereafter bonding the surface of the first substrate to the oxide on the non-recessed surface of the first silicon portion.

19. The method of claim 1 wherein the functional element is connected to two metal leads within the recessed cavity.

20. A method for packaging a MEMS device comprising:

providing a first substrate and a second substrate, the second substrate comprising an SOI wafer having a first silicon portion, a second silicon portion and an oxide portion therebetween;

forming a functional element on a surface of the first substrate;

forming at least two metal leads on the surface of the first substrate, wherein at least one of the metal leads connects to the functional element;

etching at least one recessed cavity in the first silicon portion of the second substrate;

forming at least two metal connectors in the at least one recessed cavity for connecting to a respective metal lead on the surface of the first substrate wherein the recessed cavity is etched to a depth greater than the thickness of the functional element and less than the combined thickness of the metal connectors and respective metal leads;

bonding the surface of the first substrate to a non-recessed surface of the first silicon portion and bonding each metal connector to the respective metal lead thereby sealing the functional element in the at least one recessed cavity;

removing the second silicon portion of the second substrate thereby exposing the oxide portion;

etching a via through the oxide portion and the first silicon portion over each metal connector to expose at least a portion of each metal connector; and

forming a metal pad on the exposed portion of each metal connector in the via.

21. The method of claim 20 further comprising, after forming the metal pads, depositing a passivation layer on the exposed oxide portion and metal pads.

22. The method of claim 21 wherein depositing the passivation layer includes plasma enhanced chemical vapor deposition with a nitrogen-containing reactant to deposit a nitride passivation layer.

23. The method of claim 20 wherein bonding comprises room temperature fusion bonding.

24. The method of claim 23 wherein the fusion bonding includes applying a pressure in the range of about 800-1400 pounds.

25. The method of claim 23 wherein the first substrate is a silicon base wafer.

26. The method of claim 20 wherein bonding comprises anodic bonding.

27. The method of claim 26 wherein the anodic bonding comprises applying an electrical bias in the range of about 100-1000 V and a temperature in the range of about 300-500°C.

28. The method of claim 26 wherein the first substrate is a Pyrex glass base wafer.

29. The method of claim 20 wherein the metal leads and the metal connectors each comprise a metal selected from the group consisting of: aluminum, gold, aluminum alloys and gold alloys.

30. The method of claim 29 wherein the metal leads and connectors comprise the same metal.

31. The method of claim 20 wherein the forming metal pads comprises depositing aluminum on a titanium/titanium nitride liner.

32. The method of claim 20 wherein the forming metal pads comprises depositing gold on a chromium liner.

33. The method of claim 20 wherein the SOI wafer comprises a plurality of recessed cavities in the first silicon portion, each having at least one metal connector therein for bonding to a respective metal lead, the functional element and connected metal lead bonded to the respective metal connector being enclosed and sealed within one of the plurality of cavities, and the metal pads on each of the metal connectors connecting over the oxide portion of the SOI wafer to electrically connect the functional element within one cavity to the metal lead in another cavity.

34. The method of claim 33 further comprising forming a plurality of functional elements, each enclosed and sealed within one of the plurality of cavities.

35. The method of claim 20 further comprising, before bonding, growing an oxide on the non-recessed surface and in the recessed cavity of the first silicon portion, and thereafter bonding the surface of the first substrate to the oxide on the non-recessed surface of the first silicon portion.

36. The method of claim 20 wherein the functional element is connected to each of the at least two metal leads.

37. A MEMS package comprising:

a first wafer having at least one functional element and at least two metal leads thereon, at least one of the two metal leads being connected to the functional element;

a second wafer having a silicon portion, a silicon oxide portion, at least one recessed cavity in the silicon portion, and at least two metal connectors in the recessed cavities;

a first bond between a non-recessed surface of the silicon portion of the second wafer and the first wafer wherein the at least one recessed cavity is hermetically sealed thereby, and wherein the functional element and connected metal lead of the first wafer are enclosed within the at least one recessed cavity of the second wafer and hermetically sealed therein, and wherein the depth of the recessed cavity is greater than the thickness of the functional element; and

a second bond between each of the at least two metal connectors of the second wafer and a respective one of the at least two metal leads of the first wafer;

a metal pad connected to each metal connector of the second wafer through the silicon oxide portion and silicon portion.

38. The package of claim 37 wherein the functional element of the first wafer is connected to two of the at least two metal leads of the first wafer, and the functional elements and two connected leads are enclosed within the at least one recessed cavity of the second wafer.

39. The package of claim 37 further comprising a passivation layer on the silicon oxide portion of the second wafer and on a portion of the metal pads.

40. The package of claim 39 wherein the passivation layer is silicon nitride.

41. The package of claim 37 further comprising an oxide layer on the non-recessed surface and within the recessed cavity, wherein the first bond is between the oxide layer on the non-recessed surface and the first wafer, and wherein the at least two metal connectors are on the oxide layer within the recessed cavity.

42. The package of claim 37 wherein the first wafer is a silicon base wafer.

43. The package of claim 37 wherein the first wafer is a Pyrex glass base wafer.

44. The package of claim 37 wherein the metal leads and the metal connectors each comprise a metal selected from the group consisting of: aluminum, gold, aluminum alloys and gold alloys.

45. The package of claim 44 wherein the metal leads and connectors comprise the same metal.

46. The package of claim 37 wherein the metal pads comprise aluminum on a titanium/titanium nitride liner.

47. The package of claim 37 wherein the metal pads comprise gold on a chromium liner.

48. The package of claim 37 wherein the second wafer comprises a plurality of recessed cavities in the silicon portion, each having at least one metal connector therein, the functional element being enclosed and sealed within one of the plurality of cavities, and the metal pads on each of the metal connectors connecting over the oxide portion.

49. The package of claim 48 further comprising a plurality of functional elements, each enclosed and sealed within one of the plurality of cavities.

50. The package of claim 37 wherein the functional element is connected to two metal leads within the recessed cavity.